SIGMA-DELTA ANALOG TO DIGITAL CONVERTER ARCHITECTURE BASED UPON A MODULATOR DESIGN EMPLOYING A MIRRORED INTEGRATOR

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ABSTRACT

We present a method to increase the resolution and stability of ΣΔ analog to digital converters in which the entire ΣΔ modulator is enclosed in a chopper-stabilization (CHS) structure. Simulations of the proposed architecture show that the effects of integrator opamp non-idealities (1/f noise, DC offset and drift) and digital-to-analog converter (DAC) DC offset and even-order distortion harmonics are eliminated and that the effect of integrator saturation distortion is reduced by up to 27dB in comparison to existing designs. Finally, the proposed architecture may be realized in a single-ended design enabling area-conservative circuit layouts.

1. INTRODUCTION

There are two fundamentally distinct A/D conversion approaches, Nyquist-rate converters, which offer low-to-moderate resolution and high-bandwidth and over-sampling converters, particularly those employing ΣΔ modulation, which have high-resolution and low-to-moderate bandwidth. There are several distinct advantages of the ΣΔ ADC architecture: system integration is simplified by reducing the burden on the supporting analog circuits (antialias filters and sample-and-hold circuitry) and the ΣΔ architecture is tolerant of component mismatch. Furthermore, the scaling in modern VLSI has created greater opportunities for ΣΔ converters, which derive their performance from the components’ speed in contrast to Nyquist-rate ADCs in which performance derives from the components’ precision.

In the context of ΣΔ ADC’s there are three ways to improve the resolution-bandwidth (RBW) product: increase the over-sampling ratio (OSR), increase the modulator order, or increase the quantizer resolution. Increasing the OSR is the most straightforward approach for improving the RBW product. However, the benefits from further OSR increases are likely to be moderate at best. Furthermore, one-bit ΣΔ modulators have proven to be unstable for modulator orders higher than second. Cascaded structures that increase the modulator order have been reported [1], but in such designs component mismatch emerges as a limiting factor. Therefore, further RBW product increase is most likely to come from multi-bit quantizer designs, [2]. However, nonlinearities in multi-bit DAC’s lead to nonlinear ADC signal response and the resulting signal harmonic distortion limits the converter’s effective dynamic range. Various design approaches have been used to address the DAC non-linearity problem. Additional non-idealities such as 1/f noise, dc offset and dc drift of the integrator opamp and DAC also limit ΣΔ ADC performance. The chopper stabilization (CHS) method, described in [3], may eliminate the effects of most of the integrator opamp non-idealities. However, these CHS methods have focused only on the integrator opamp in the ΣΔ structure.

We propose a general structure in which the entire ΣΔ modulator is enclosed with a CHS structure, as shown in Fig. 1. A specific 2nd order implementation of this general approach was proposed in [4]. In the proposed architecture the modulator filters would be Mirrored Integrators (MI) thus we refer to the entire structure as a Mirrored-Integrator-ΣΔ modulator (MISD).

2. MISD MODULATOR SYSTEM DESIGN

In the proposed approach the input signal is shifted near the Nyquist frequency, by employing a square-wave chopper operating at a frequency f_s/2, where f_s is the sampling frequency.
In the MISD design the ΣΔ modulator shapes the quantization noise toward the low frequency portion of the spectrum as opposed to conventional ΣΔ modulators in which the quantization noise is shaped toward the high frequency region of the spectrum [5].

Figure 2 presents a more detailed view of the Nth order MISD architecture. In contrast to conventional designs the feedback signal is added to the input signal and in place of an integrator the mirrored integrator is used. The general form of the MI discrete-time transfer function is given in Eq. (1), where i=1,2,3…N.

\[ H_{MI}(z^{-1}) = \frac{H_i(z^{-1})(B_{i,0} + B_{i,1}z^{-0.5} + B_{i,2}z^{-1})}{1 + z^{-1}} \]  

(1)

To illustrate the noise shaping property of the MISD structure, a first-order MISD will be considered (N=1, A1=1, B0=0, B1=0, and B2=1), shown in Fig. 3. The output signal from the quantizer of the first-order MISD is given by Eq.(2).

\[ Y(z^{-1}) = H_{e}(z^{-1}) \cdot E(z^{-1}) + z^{-1}X(z^{-1}) \]  

(2a)

\[ H_{e}(z^{-1}) = (1 + z^{-1}) \]  

(2b)

where \( E(z^{-1}) \) is the linear representation of the quantization noise, and \( X(z^{-1}) \) is the sign-alternated input signal. Thus, the sign-alternated input signal is simply delayed and the quantization noise \( E(z^{-1}) \) is shaped toward the low-frequency portion of the spectrum. After high-pass filtering, the modulated input signal remains the same, but the excess noise, i.e., the noise in the lower frequency portion of the spectrum, is removed.

The output signal from the MISD modulator is demodulated back to base-band by multiplying by the same chopper signal and passing through a low-pass decimation filter, as shown in Fig. 1, or alternatively by a high-pass decimation filter without demodulation. In contrast to conventional ΣΔ designs employing CHS, the chopper that is used at the output of the amplifier to demodulate the output signal is moved outside the ΣΔ loop. This reduces the charge injection at the amplifier’s output node.

2.1. Mirrored Integrator realization and noise analyzes

The block diagrams of the sample-delayed and non-delayed mirrored integrators are shown in Fig. 4.

The MI can be realized in both fully-differential, [6], and single-ended switched-capacitor circuit designs. Although the fully differential design is preferred in conventional ΣΔ ADC’s, in this paper we focus on the single-ended design to demonstrate that the MISD concept will enable area efficient low-noise design with existing single-ended amplifiers with noise performance similar to fully-differential amplifiers employing CHS. Single-ended designs are more area efficient than fully-differential designs because there is no need for a common-mode-feedback circuit. Furthermore, single-ended designs avoid cross-path component mismatch, which is a design challenge in fully-differential designs. Although, the design proposed in [7] may be used in both the conventional and MISD single-ended designs, it suffers from low output voltage headroom, which becomes more of a factor in modern low-voltage CMOS designs. A possible single-ended realization of the MI with proper timing sequence is shown in Fig. 5, where \( e[n] \) represents the additive opamp noise. A half-sample delay in \( \phi_1 \) and \( \phi_2 \) is required to avoid charge injection. The discrete-time transfer function of the MI is given in Eq. (3).

\[ H_{MI}(z^{-1}) = -\frac{C_1}{C_2} \frac{z^{-1}}{1 + z^{-1}} \]  

(3)

In order to estimate the input referred opamp noise, the input signal is assumed to be equal to zero. The resulting noise transfer function is given in Eq (4).

\[ H_{e}(z) = \frac{V(z)}{E(z)} = \frac{1 + \frac{C_1}{C_2} z^{-0.5} + z^{-1}}{1 + z^{-1}} \]  

(4)
Figure 5: Sample-delayed single-ended MI realization

From Eq. (4), the opamp noise undergoes linear filtering without modulation. Thus, although filtered, the opamp 1/f noise and DC offset remain in the lower portion of the spectrum and do not corrupt the input signal that was shifted near the Nyquist frequency. When referred to the MI input, the opamp thermal noise, which is white noise for all realizable sampling frequencies, undergoes low-pass filtering given by the transfer function in Eq. (5), where \( \omega \) represents digital frequency.

\[
H_{in}(j\omega) = -(1 + \exp(-j\omega))
\]

The thermal noise power near the Nyquist frequency, \( \omega = \pi \), is highly attenuated resulting in improved signal to noise ratio. The foregoing analysis shows that proposed single-ended MI reduces the opamp noise as well as a fully differential integrator employing CHS.

### 2.2. Simulation results

For the simulations presented below, a second-order, 4-bit MISD structure was employed. A 10Hz, -6dB input signal lying within a 50Hz signal bandwidth was assumed. A sampling frequency of 2 kHz was used (OSR=20).

**DAC non-idealities:** Due to inherent linearity of the single-bit DAC, the single-bit MISD design has no advantages over the conventional designs in terms of suppressing DAC nonlinearities, except that it removes the DC offset of the single-bit DAC that is always present due to component mismatch. However, when a multi-bit structure is employed, it has been shown that the harmonic distortion caused by a multi-bit DAC become the dominant limiting factor of the signal-to-noise + distortion ratio (SNDR) and the dynamic range. The DAC output is directly coupled to the input signal, thus all DAC non-idealities pass through the conventional \( \Sigma\Delta \) modulator with no change thus degrading the input signal. On the other hand, in multi-bit MISD designs, the DAC output is coupled to the frequency-shifted input signal. As a result, all even-order harmonic distortions including the DC offset are folded back to DC and thus removed by the high-pass filter.

The odd-order harmonics fold back to the Nyquist frequency and thus contribute to degradation to the SNR although simulations indicate that this degradation is less than in conventional \( \Sigma\Delta \) designs. For simulation purposes, it was assumed that the DAC nonlinear transfer function may be represented by a polynomial as shown in Eq. (6). The coefficients \( a_1 \) and \( a_2 \) are chosen to maintain a DAC effective linearity of approximately 10-bits.

\[
y[n] = x[n] + a_1 x^2[n] + a_2 x^3[n] \quad (6)
\]

For coefficient values of \( a_1=0.0008 \) and \( a_2=0.0004 \), as seen in Fig. 6, the noise + distortion power is reduced by 16.73dB in the MISD design, resulting in an overall ADC effective resolution improvement of 2.8 bits.

The ability of the MISD architecture to remove low-frequency non-idealities leads to a reduction of the DAC nonlinearity ill effects. Extensive analyses of various multi-bit DAC designs have been conducted and the presence of the significant even-order harmonic power has been confirmed, so a significant improvement in ADC resolution is expected for the MISD structure.

**MI non-idealities:** Our simulations have confirmed that the MI’s DC offset and 1/f noise are removed, and that thermal noise is attenuated. Another important improvement achieved by the MISD design is suppression of the nonlinearity caused by single-side clipping, which leads to an improvement of SNR and stability. In practice, the integrator and MI have a finite output voltage swing. When the input signal increases, causing the opamp output to approach the power supply rails of the opamp, clipping distortion appears which limits the maximum SNR and eventually causes instability, see Fig. 8. If the opamp rails are placed symmetrically around the output common-mode voltage value, the MISD design has no advantage over conventional designs. However, due to process variations, the ideal situation is seldom realized, and therefore the reduced sensitivity to clipping of the MI may lead to improvements. In order to present the improvements, an input signal with DC component of 0.2V and AC component of 0.8V was assumed.
The opamp rails were assumed to be equal to \( V_{\text{max}} = 0.96\text{V} \) and \( V_{\text{min}} = -1.04\text{V} \) (2% rail error). Thus, positive-side clipping is more likely to occur. The resulting output spectrum is shown in Fig. 7. The total distortion power in the 50Hz signal bandwidth of the MISD design is 27dB lower than in the conventional \( \Sigma \Delta \) design. In order to determine the best achievable SNR, the input signal ac amplitude was swept from 0.5V to 1V. A SNR was calculated under the same opamp rail conditions assumed above. From Fig. 8 we see that the maximum SNR improvement of the MISD is not more than 3dB (0.5bits), which is not a significant improvement in effective resolution. The maximum SNR is nearly identical in the conventional and MISD architectures, however the SNR decreases more slowly in the MISD design thus reducing the probability that the MISD would become unstable. The end result may be an overall stability improvement over conventional designs. This statement is based upon the assumption that the high power distortion, added to an already large input signal, might saturate the opamp leading to instability.

**Quantizer non-idealities**: In higher-order and/or higher OSR designs, multi-bit quantizer ill effects (DC offset, non-linear transfer function and clipping) are highly suppressed by the noise transfer function and thus may be neglected in comparison to the DAC non-idealities. However, in applications where the OSR is low (due to limited speed and/or large input signal bandwidth) and the modulator order is low (due to area constraints and/or reduced power consumption), the quantizer ill effects become visible above the noise floor. Thus, in low OSR, low-order, multi-bit designs, the quantizer non-idealities must be addressed. The simulations have shown that, similar to DAC non-idealities, the MISD structure removes even-order distortions that are generated by nonlinearity in a multi-bit quantizer transfer function. Also, non-symmetric rails of the multi-bit quantizer reduce the maximum signal power that can be handled by the ADC, a problem for which the MISD structure again offers improvement over the conventional designs.

### 3. CONCLUSIONS

A general \( \Sigma \Delta \) modulator architecture based on the mirrored integrator has been proposed and analyzed. Simulations demonstrate that this architecture improves the effective resolution and relaxes the stability requirements by attenuating non-linear effects. Also, a single-ended loop filter design has been proposed allowing more compact \( \Sigma \Delta \) layouts. In an ongoing effort we are seeking to demonstrate the promised advantages of the MISD through tests of fabricated circuits.

### 4. REFERENCES


